Enhancing p-channel InGaSb QW-FETs via Process-Induced Compressive Uniaxial Strain

Luke W. Guo, Ling Xia, Brian R. Bennett, J. Brad Boos, Mario G. Ancona, and Jesús A. del Alamo, *Fellow, IEEE*

***Abstract*— We study the effect of process-induced uniaxial stress on the performance of biaxially strained InGaSb p-channel quantum-well field-effect transistors (QW-FETs). Uniaxial stress is incorporated using a self-aligned nitride stressor. Compared with unstressed control devices, fabricated stressed devices with a gate length of $L_g = 0.30$ μm showed an increase of more than 40% in the drain current at V_{GS}–V_T = −0.5 V and V_{DS} = −2.0 V, an enhancement of more than 40% in the peak extrinsic transconductance at V_{DS} = −2.0 V, and a reduction in the source and drain resistance of 25%. These figures suggest an enhancement of the intrinsic transconductance by as much as 60%. The improvement in device characteristics was also found to scale favorably with gate length. The results indicate that process-induced compressive uniaxial strain holds great promise for developing high-performance antimonide-based p-FETs.**

***Index Terms*— Antimonide, QW-FETs, InGaSb, p-FET, stressed dielectric, uniaxial strain.**

I. Introduction

As CONCERNS grow over the feasibility of scaling silicon CMOS devices to the nanometer regime, III-V channels have shown great promise as candidates for integration into future-generation logic devices due to their outstanding electron transport properties [1]. However, while impressive III-V n-FETs have been demonstrated [2]–[4], this success has not yet been translated to III-V p-FETs, due to a generally lower hole mobility. Amongst all III-V materials, the antimonide system has the highest hole mobility, making it a likely candidate for the development of high performance III-V p-FETs [5].

One approach to enhance p-type device performance is to add compressive strain, which found widespread use in high-volume silicon manufacturing [6]. By incorporating compressive biaxial strain during epitaxial growth, antimonide heterostructures with hole mobilities as high as 1500 $cm^2/V{\cdot}s$ have been demonstrated [7]. Antimonide p-FETs have also been fabricated using biaxially strained heterostructures [8]–[10]. The effect of uniaxial strain on biaxially strained antimonide p-FETs has been studied through chip-bending experiments [11]. The study showed that the superposition of uniaxial and biaxial stress can add super-linearly to enhance the performance of antimonide devices. However, the amount of uniaxial stress that can be applied via chip-bending experiments has been limited to <50 MPa. On the other hand, process-induced techniques can be used to achieve significantly larger stress levels. While the superposition of grown biaxial strain and process-induced uniaxial strain has been shown to enhance the transport performance of GaAs/InGaAs p-FETs [12], [13], such a study has yet to be performed for antimonide-based p-FETs.

In this letter, we study the effect of adding process-induced uniaxial strain on biaxially-strained InGaSb p-type QW-FETs through the use of a compressively stressed nitride layer. Compressively stressed devices show a significant increase in drain current and transconductance and a reduction in parasitic resistance over that of unstressed devices.

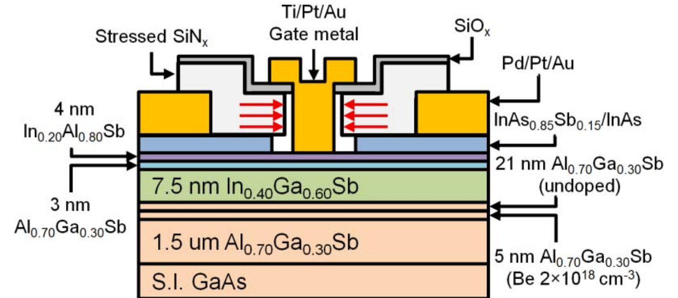

Fig. 1. Device structure used in this letter. It features a self-aligned nitride layer that applies compressive stress (indicated by red arrows) to the intrinsic region of the device to enhance device performance.

II. Device Fabrication

Fig. 1 shows a cross-section of the device. The heterostructure was grown by molecular beam epitaxy on a semi-insulating GaAs substrate. Growth of the structure began with a relaxed $Al_{0.70}Ga_{0.30}Sb$ buffer 1.5 μm thick, followed by a 5 nm layer doped with a Be concentration of 2×10^{18} cm^{-3} and 21 nm of undoped $Al_{0.70}Ga_{0.30}Sb$. Then, a 7.5 nm $In_{0.40}Ga_{0.60}Sb$ channel layer under −2% compressive biaxial strain is grown along with a 7 nm thick barrier comprised of 3 nm of $Al_{0.70}Ga_{0.30}Sb$ and 4 nm of $In_{0.20}Al_{0.80}Sb$. Finally, the heterostructure is capped off by a highly-doped bilayer of $In_{0.85}As_{0.15}Sb$ (30 nm) with InAs (5 nm) on top with a Be concentration of 10^{19} cm^{-3}.

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L. W. Guo, L. Xia, and J. A. del Alamo are with Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: lukeguo@mit.edu).

B. R. Bennett, J. B. Boos, and M. G. Ancona are with the Electronics Science and Technology Division, Naval Research Laboratory, Washington, DC 20375 USA.

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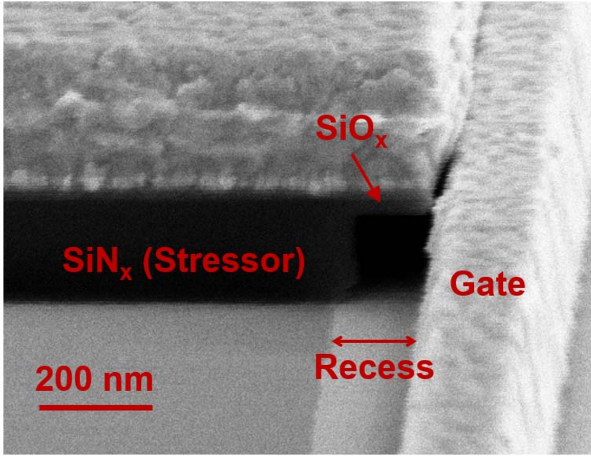

Fig. 2. SEM image showing the edge of the self-aligned nitride stressor. After etching through the nitride, the highly-doped cap layer is recessed and the Ti/Pt/Au gate metal is deposited and patterned using lift-off.

Pd/Pt/Au ohmic contacts are first formed using electron beam deposition and lift-off. The contacts are subsequently annealed at 200°C in N_2/Ar for 3 hours. A −1.5 GPa compressively stressed silicon nitride (SiN_x) dielectric layer with a thickness of 160 nm is then deposited via PECVD, followed by 50 nm of silicon dioxide as a protective layer. A narrow opening is defined by electron beam lithography and the composite dielectric is patterned using SF_6/O_2 plasma etching. After wet recess of the $InAs/In_{0.85}As_{0.15}Sb$ cap bilayer using a 3:1 citric acid (1 gm/mL) to H_2O etchant solution, a Ti/Pt/Au metal gate stack is deposited and patterned using lift-off. Finally, a mesa etch is used for device isolation, creating a gate air-bridge. A control sample is fabricated in parallel and is identical in every way except that the deposited nitride layer is stress-free. Devices with gate lengths of 0.30, 0.47, and 0.67 μm were fabricated, with gate widths of 25 μm and a source-drain separation of 2 μm. Devices with carrier transport along the [110] orientation are studied.

When an opening in the nitride layer is created to accommodate the gate, the semiconductor region located near the edge of the nitride film experiences high compressive stress. As the dimension of the opening decreases, the magnitude of the stress in the channel region underneath the gate increases. Mechanical simulations suggest that enhancements of more than 160% can be achieved with gate lengths <50 nm [13]. Our device architecture features a self-aligned stressor, allowing the edge of the nitride layer to be in very close proximity to the intrinsic channel region. Fig. 2 shows a SEM image of a completed device and reveals a tight ∼150 nm spacing between the gate edge and cap edge, which is determined by the edge of the nitride layer and the wet recess. Consequently, this self-aligned device architecture offers promising scalability and an excellent framework to study the effect of process-induced uniaxial stress on InGaSb p-FETs.

III. Results and Discussion

A significant enhancement in device performance was observed in the stressed devices. The left graph of Fig. 3 shows the output characteristics of both a uniaxially stressed

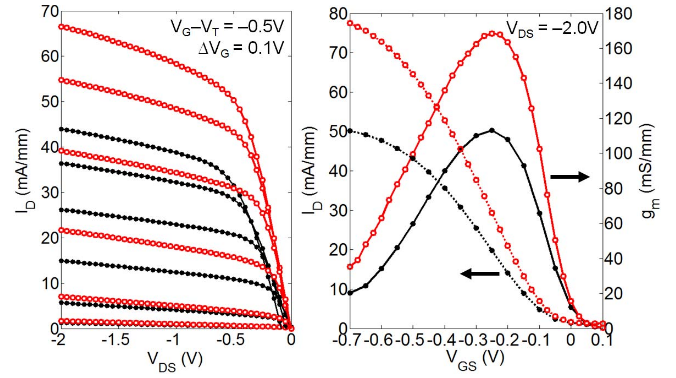

Fig. 3. (Left) Output characteristics of stressed (red) and unstressed (black) devices for $L_g = 0.30$ μm. (Right) Extrinsic transconductance (solid) and drain current (dashed) of the devices at $V_{DS} = -2.0$ V.

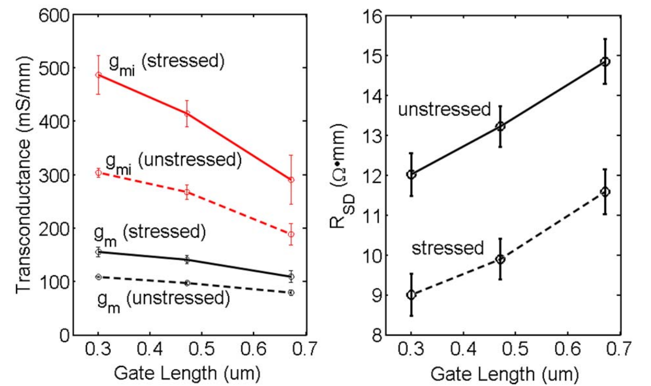

Fig. 4. (Left) Extrinsic and intrinsic transconductance as a function of gate length for InGaSb p-FETs. (Right) Source-drain resistance shown as a function of gate length. The bars indicate the error of ∼5 devices.

and unstressed InGaSb p-FET with $L_g = 0.30$ μm. At $V_{GS} - V_T = -0.5$ V and $V_{DS} = -2.0$ V, the stressed device shows 40% more drain current than the unstressed device. A significant enhancement in the transconductance, g_m, for the stressed device is also observed, as shown on the right of Fig. 3. For the stressed and unstressed devices, the peak g_m is 168 mS/mm and 113 mS/mm, respectively, giving an increase of more than 40%.

The left plot of Fig. 4 shows the dependence of g_m and the intrinsic transconductance, g_{mi}, on L_g. g_{mi} was determined using the output conductance, as well as the source and drain resistances [14], which were measured using the gate current injection method [15]. Average enhancements of 60%, 48%, and 33% in g_{mi} were seen for devices with $L_g = 0.30$, 0.47, and 0.67 μm, respectively. The amount of g_{mi} enhancement increases as L_g is scaled down, consistent with mechanical simulations of the stress distribution [13].

The effect of stress on the source-drain resistance, R_{SD}, was also studied as a function of gate length and is shown on the right of Fig. 4. Stressed devices showed lower R_{SD} than unstressed devices for every gate length. For $L_g = 0.30$ μm, R_{SD} decreased from 12.0 ± 0.6 Ω·mm for unstressed devices to 9.0 ± 0.5 Ω·mm for stressed devices, giving an average reduction of 25%. The bars in these figures represent the error of ∼5 devices, indicating statistical significance of all

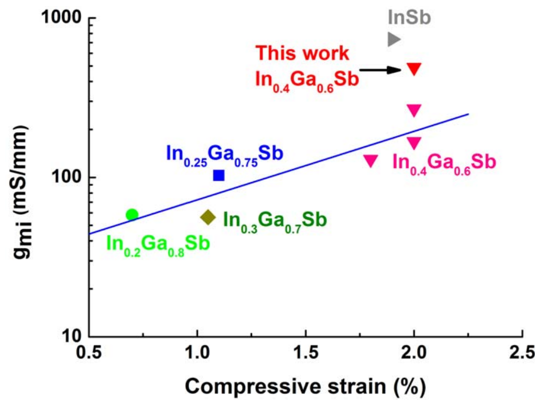

Fig. 5. Intrinsic transconductance as a function of compressive biaxial strain in the as-grown channel. The performance of our uniaxially enhanced devices approaches that of pure InSb channel p-FETs with much shorter gate length [8]–[10], [16]–[20].

our results. The reduction in R_{SD} was also observed in InGaAs p-FETs [13] and is attributed to the high compressive stress that is induced in the access regions near the edge of the silicon nitride film.

This letter shows that by combining process-induced uniaxial stress with biaxial stress incorporated via epitaxial growth, a large enhancement in device performance can be achieved in InGaSb p-FETs. Enhancements as high as 60% in g_{mi} obtained in this letter are significantly higher than those observed earlier in InGaAs p-FETs (36%). In addition, the overall performance of our InGaSb p-FETs compares favorably with other devices in literature. Fig. 5 graphs g_{mi} against compressive biaxial strain in the as-grown channel, a dominant factor affecting hole mobility and transistor performance. Different channel compositions are labeled. For the same as-grown channel strain, the addition of uniaxial strain in our devices substantially enhances g_{mi}. In fact, the performance of our devices approaches that of pure InSb channel p-FETs with much shorter gate length [9].

IV. Conclusions

We have demonstrated that the incorporation of process-induced compressive uniaxial stress to InGaSb QW-FETs with a biaxially compressed channel substantially increases the transport related figures of merit of submicron devices. With device scaling, optimization of the dielectric stressor, and reduction of the parasitic resistance, even larger enhancements are to be expected. The results show that the use of process-induced uniaxial stress holds great promise for enhancing InGaSb p-FETs for future CMOS applications.

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